

USED ON A7201

ETJ SETS UP APPROPRIATE SCR OR B REGISTER ADDRESS IN I REGISTER AS FOLLOWS

PRIORITY LEVEL	E1	E2	J3	J2	J1	
					FOR SCR	FOR B REG
1 (HIGHEST)	0	0	0	0	0	1
2	1	0	0	1	0	1
3	0	1	1	0	0	1
4 (LOWEST)	1	1	1	1	0	1

KTJ SETS UP J REGISTER FOR MULTIPLICATION AND DIVISION AS FOLLOWS

FUNCTION	J5	J2	J1
13	1	1	0

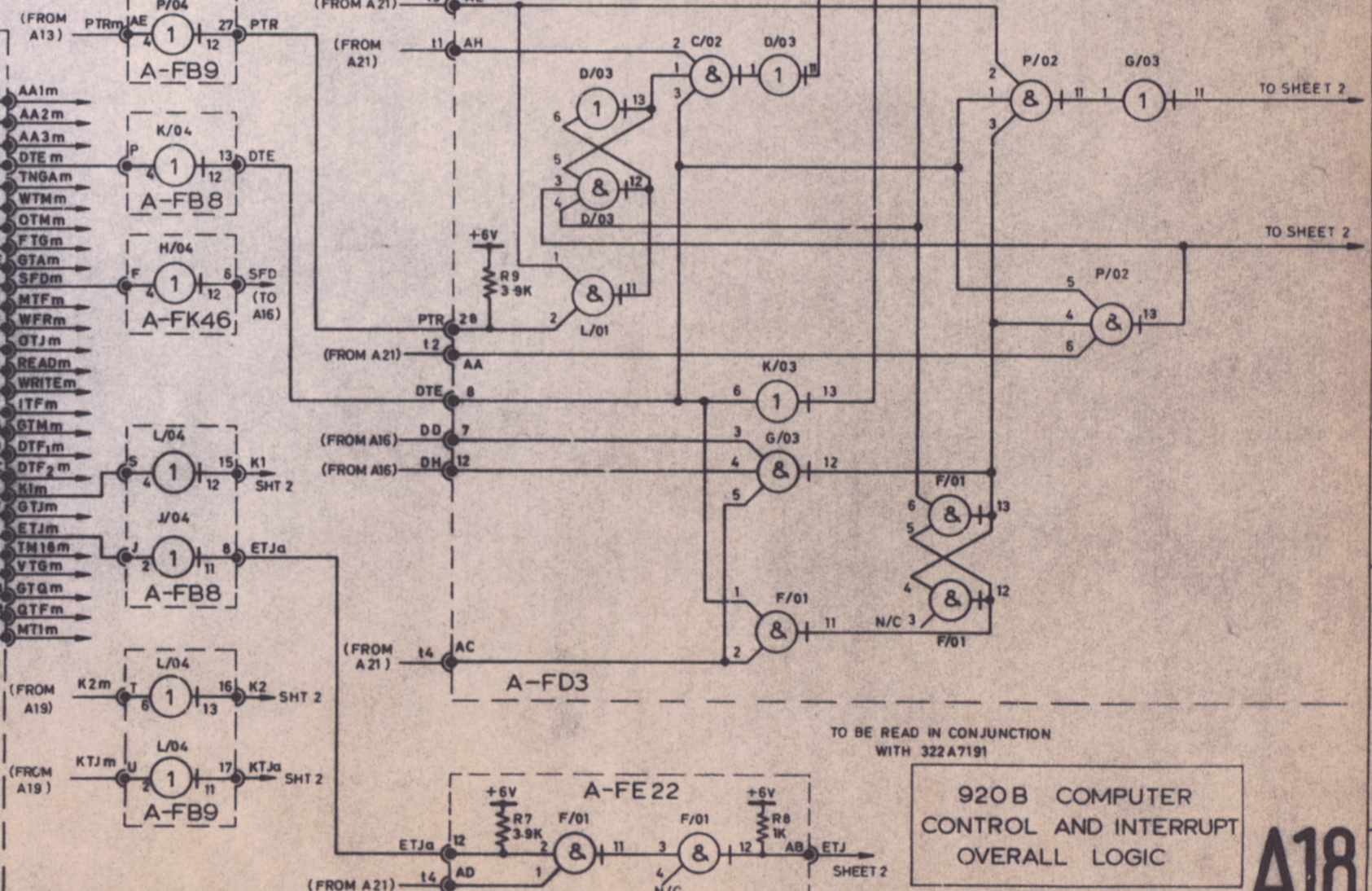
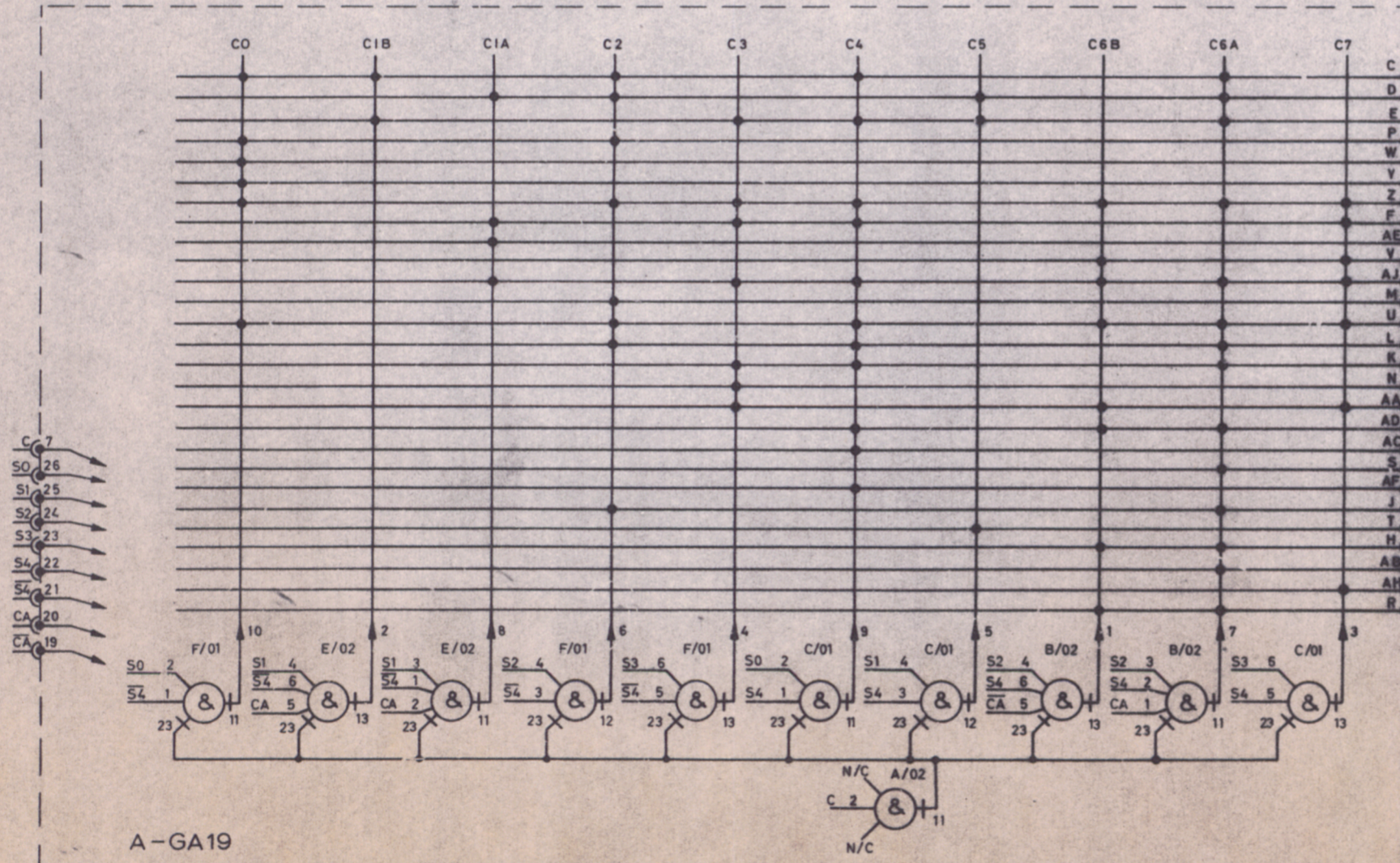
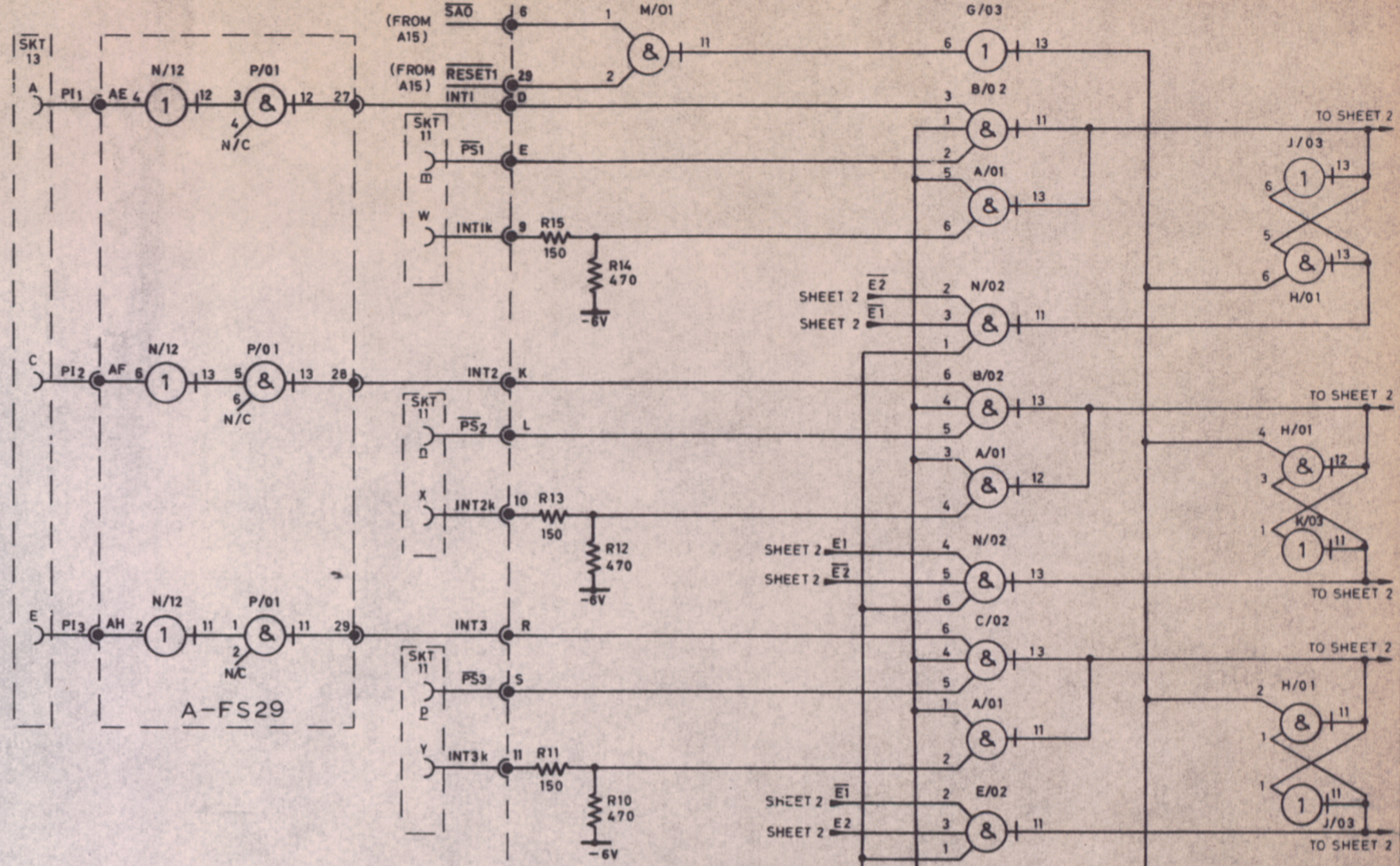
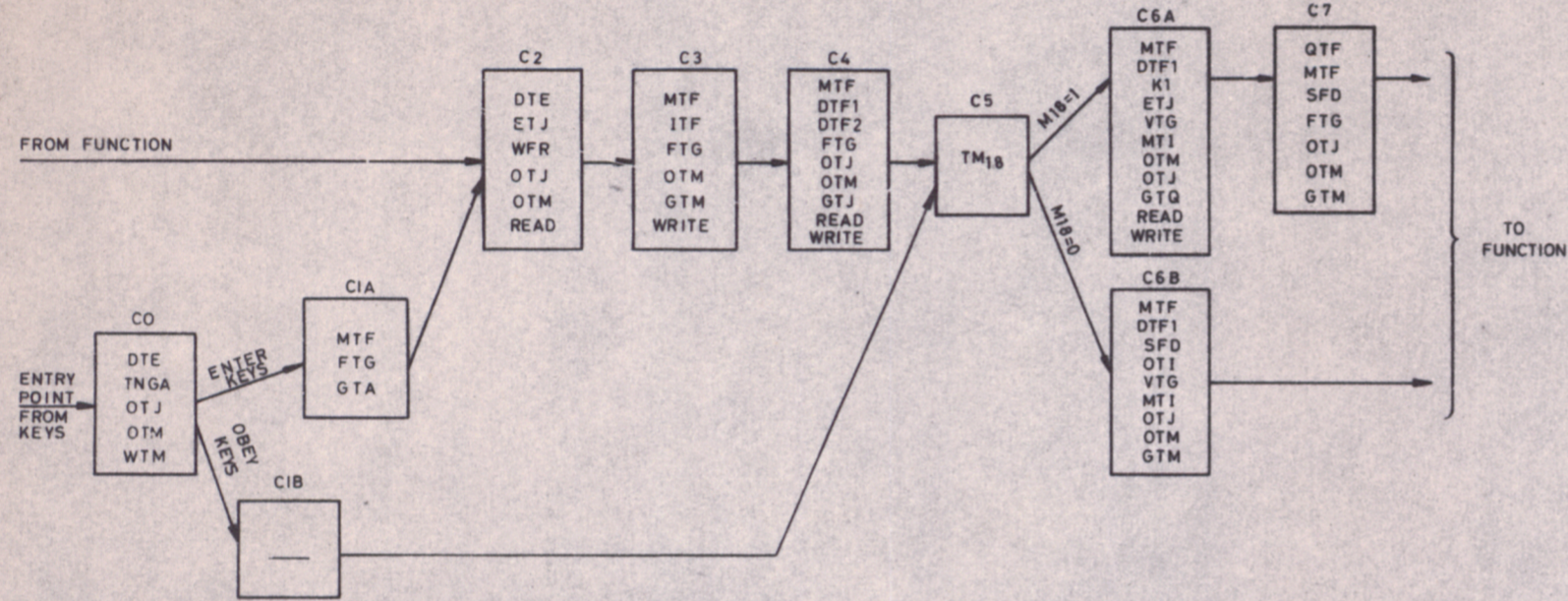
J REG SET UP BY

KTJ <sub>5</sub>	ETJ <sub>2</sub> FROM KTJ WHEN K2 = 1	KTJ <sub>1</sub> FROM KTJ WHEN K2 = 0
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J. REG. SET UP BY

ETJ <sub>3</sub>	ETJ <sub>2</sub>
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KTJ<sub>1</sub> FROM ETJ AND K1 = 1



TO BE READ IN CONJUNCTION WITH 322A7191

920B COMPUTER CONTROL AND INTERRUPT OVERALL LOGIC

SHT 1 OF 2

A18

LATEST M.I. INCORPORATED M.I. 2993

ISSUE No.	1	MATERIAL	FINISH	ELLIOTT BROTHERS (LONDON) LTD
ALT <sup>n</sup> No.	1661	TOLERANCES DECIMAL & FRACTIONAL <math>^{\circ}</math> ANGULAR DIMENSIONS <math>^{\circ}</math> UNLESS OTHERWISE STATED		TITLE 920B COMPUTER CONTROL AND INTERRUPT OVERALL LOGIC
DATE	4.1966	SCALE SHT 1 OF 2		DRAWING No. 322D 8070
INITIALS	WYP	DRAWN J.S.B. CHECKED C.B.S. APPROVED A.P.		DATE 27.5.66
PARTS LIST No.				